WHAT IS CLAIMED IS:

1. A bus agent comprising:

a control interface to drive a control signal at a clock frequency;

an address bus interface to drive address elements at twice the clock frequency, said address bus interface to drive a substantially centered address strobe transition for each address element;

a data bus interface to drive data elements at four times the clock frequency, said data bus interface to drive a substantially centered data strobe transition for each data element.

2. The bus agent of claim 1 wherein said data bus interface is to generate first, second, third, and fourth data elements in a first signal generation time period and wherein said address bus interface is to generate first and second address elements in a second signal generation time period, said first signal generation time period and said second signal generation time period each being substantially equivalent to a clock cycle of a clock signal that operates at the clock frequency, wherein:

a first edge of a first data strobe is to be positioned at approximately a 12.5 percent point of the first signal generation time period;

a first edge of a second data strobe is to be positioned at approximately a 37.5 percent point of said first signal generation time period;

a second edge of said first data strobe is to be positioned at approximately a 67.5 percent point of the first signal generation time period;

a second edge of said second data strobe is to be positioned at approximately a 87.5 percent point of the first signal generation time period;

said first data element to be generated at approximately a beginning of the first signal generation time period;

said second data element is to be transmitted at approximately a twenty five percent point of the first signal generation time period;

said third data element is to be transmitted at approximately a fifty percent point of the first signal generation time period;

said fourth data element is to be transmitted at approximately a seventy five percent point of the first signal generation time period.

a first edge of a first address strobe is to be positioned at approximately a twenty five percent of said second signal generation time period,

a second edge of said first address strobe is to be positioned at approximately a seventy five percent of said second signal generation time period;

said first address elements is to be transmitted at approximately a beginning of the second signal generation time period;

said second address elements is to be transmitted at approximately a fifty percent point of the second signal generation time period.

3. The bus agent of claim 1 further comprising:

address strobe generation logic to generate a first address strobe to have a first address strobe transition at substantially a first address element center point of a first address element driving window in which a first address element is to be driven, and wherein

said address strobe generation logic is to generate said first address strobe to have a second transition at substantially a second address element center point of a second address element driving window in which a second address element is to be driven;

data strobe generation logic to generate a first data strobe to have a first transition of the first data strobe at substantially a first data element center point of a first data element driving window in which a first data element is to be driven, and wherein

said data strobe generation logic is to generate a second data strobe to have a first transition of the second data strobe at substantially a second data element center point of a second data element driving window in which a second data element is to be driven, and wherein

said data strobe generation logic is to generate a second transition of the first data strobe to have a second transition of the first data strobe at substantially a third data element center point of a third data element driving window in which a third data element is to be driven, and wherein

said data strobe generation logic is to generate a second transition of the second data strobe to have a second transition of the second data strobe at substantially a fourth data element center point of a fourth data element driving window in which a fourth data element is to be driven.

4. The bus agent of claim 3 wherein said first data strobe and said second data strobe are signals having out-of-phase waveforms that have a data strobe operating frequency when enabled of twice the clock frequency.

5. The bus agent of claim 3 wherein the first transition of the first data strobe and the second transition of the first data strobe are of a first polarity and said first data strobe has a transition of opposite polarity after the first transition of the first data strobe and before the second transition of the first data strobe.

6. The bus agent of claim 1 wherein the clock signal is a bus clock signal and wherein:

said address bus interface is to transmit address elements at a rising edge of the bus clock signal in a first bus clock cycle of the bus clock signal and additional address elements at a 50 percent point of the first bus clock cycle, and wherein

said address bus interface is to generate said first address strobe to have a first address strobe transition at a 25 percent point of the first bus clock cycle and a second

address strobe transition at a 75 percent point of the first bus clock cycle, and wherein

said data bus interface is to transmit first data elements at a second rising edge of the bus clock signal in a second bus clock cycle of the bus clock signal, second data elements at a 25 percent point of the second bus clock cycle, third data elements at a 50 percent point of the second bus clock cycle, and fourth data elements at a 75 percent point of the second bus clock cycle, and wherein

said data bus interface is to generate said first data strobe and said second data strobe to have first data strobe transitions at a 12.5 percent point of the second bus clock cycle, second data strobe transitions at a 37.5 percent point of the second bus clock cycle, third data strobe transitions at a 67.5 percent point of the second bus clock cycle, and fourth data strobe transitions at a 87.5 percent point of the second bus clock cycle.

7. The bus agent of claim 1 wherein said address bus interface is to drive a first address strobe at the clock frequency, said first address strobe having a first address strobe transition of a first polarity to be substantially centered on a first address element and a second address strobe transition of a second polarity to be substantially centered on a second address element, the second address element being consecutive to the first address element, and wherein said data bus interface is to drive four consecutive data elements and a first data strobe and a second data strobe, and wherein a first edge of a

first type of the first data strobe is to be substantially centered on a first data element, a first edge of the first polarity of the second data strobe is to be substantially centered on the second data element, a second edge of the first type of the first data strobe is to be substantially centered on the third data element, and a second edge of the first type of the second data strobe is to be substantially centered on the fourth data element.

8. The bus agent of claim 1, wherein said bus agent is to support a transaction having a plurality of phases, said plurality of phases comprising an arbitration phase, a request phase, a snoop phase, a response phase, and a data phase.

9. The bus agent of claim 1 or 2 or 3, wherein said bus agent is to support a plurality of transactions having a plurality of phases, said plurality of phases comprising an arbitration phase, a request phase, a snoop phase, a response phase, and a data phase, wherein some of said plurality of phases are optional for some transactions.

10. The bus agent of claim 9 wherein

said bus agent is capable of initiating the arbitration phase after two clocks from a prior arbitration phase and capable of receiving a block next request signal two bus clock cycles after assertion of an address strobe signal occurs and capable of responding to said block next request signal.

11. The bus agent of claim 9 or 10 wherein:

said bus agent is capable of initiating a second request phase for a second transaction in a current clock cycle two clocks after a first request phase for a first transaction by asserting a plurality of request signals and a second transaction address strobe signal for the second transaction two bus cycles after assertion of a first transaction address strobe signal for the first transaction occurs if a most recent target ready signal active and data bus busy inactive observation occurred three or more clocks prior to the current clock cycle.

12. The bus agent of claim 9 or 10 or 11 wherein:

said bus agent is capable of sensing or asserting one or more of a plurality of snoop status signals for transaction N on a plurality of snoop status interfaces during a snoop phase occurring upon a later one of:

three or more bus clock cycles of a bus clock signal after the assertion of an address strobe signal for transaction N; or

a most recent snoop phase for another transaction has been observed completed for zero or more clocks.

13. The bus agent of claim 9 or 10 or 11 or 12 wherein:

said bus agent is to track a plurality of a phases of a plurality of bus transactions on a bus which is a multi-phase pipelined bus, and said bus agent is to track a

transaction N-1 and a transaction N, wherein said bus controller is capable of asserting a response for transaction N two or more bus clock cycles after asserting a response for transaction N-1.

14. The bus agent of claim 9 or 10 or 11 or 12 wherein:

said bus agent is to track a plurality of transactions comprising a transaction N-1 and a transaction N, the bus agent being capable of asserting the target ready signal for transaction N if the bus agent is asserting the data busy signal for the transaction N-1 and deasserts the data busy signal.

15. The bus agent of claim 1 wherein said address bus interface is to drive an address strobe signal having a first transition of a first type as the substantially centered address strobe transition for a first address element and is to drive a second transition of a second type as the substantially centered address strobe transition for a second address element, said first address element and said second address element being driven in a first duration substantially equivalent to a cycle of a clock signal at the clock frequency.

16. The bus agent of claim 15 wherein said data bus interface is to drive a first data strobe and a second data strobe at twice the clock frequency.

17. The bus agent of claim 16 wherein a first data strobe transition of a first data strobe transition type of the first data strobe is to be generated substantially centered to a first data element, and wherein a first data strobe transition of the first data strobe transition type of the second data strobe is to be generated substantially centered to a second data element, and wherein a second data strobe transition of the first data strobe transition type of the first data strobe is to be generated substantially centered to a third data element, and wherein a second data strobe transition of the first data strobe transition type of the second data strobe is to be generated substantially centered to a fourth data element, said first through fourth data elements being transmitted sequentially in order of the first through the fourth, said first through fourth data elements being generated in a second duration substantially equivalent to the clock cycle of the clock signal at the clock frequency.

18. The bus agent of claim 17 wherein the first type of transition is a falling edge of a data strobe.

19. A bus agent comprising:

a plurality of data pins;

a plurality of data strobe pins;

a plurality of address pins;

an address strobe pin;

a common clock pin for a bus clock signal having a bus clock frequency;

data strobe generation logic to generate a first data strobe and a second data strobe on a first data strobe pin and a second data strobe pin, said first data strobe and said second data strobe having a data strobe frequency of twice said bus clock frequency;

address strobe generation logic to generate a first address strobe on said address strobe pin having an address strobe frequency which is the same as said bus clock frequency;

data transmit logic to transmit first data elements synchronized to a first edge of said first data strobe on said plurality of data pins and to transmit second data elements synchronized to a first edge of said second data strobe also on said plurality of data pins and to transmit third data elements synchronized to a second edge of said first data strobe on said plurality of data pins and to transmit fourth data elements synchronized to a second edge of said second data strobe also on said plurality of data pins;

address transmit logic to transmit first address elements synchronized to a first edge of said first address strobe on said plurality of address pins and to transmit second address elements synchronized to a second edge of said first address strobe also on said plurality of address pins.

20. The bus agent of claim 19 wherein said first through fourth data elements are generated in a first signal generation time period and wherein said first and second address elements are generated in a second signal generation time period, said first signal generation time period and said second signal generation time period each being substantially equivalent to a clock cycle of the bus clock signal, wherein:

said first edge of said first data strobe is to be positioned at approximately a 12.5 percent point of the first signal generation time period;

said first edge of said second data strobe is to be positioned at approximately a 37.5 percent point of said first signal generation time period;

said second edge of said first data strobe is to be positioned at approximately a 67.5 percent point of the first signal generation time period;

said second edge of said second data strobe is to be positioned at approximately a 87.5 percent point of the first signal generation time period;

said first data elements to be generated at approximately a beginning of the first signal generation time period;

said second data elements is to be transmitted at approximately a twenty five percent point of the first signal generation time period;

said third data elements is to be transmitted at approximately a fifty percent point of the first signal generation time period;

said fourth data elements is to be transmitted at approximately a seventy five percent point of the first signal generation time period.

said first edge of said first address strobe is to be positioned at approximately a twenty five percent of said second signal generation time period,

said second edge of said first address strobe is to be positioned at approximately a seventy five percent of said second signal generation time period;

said first address elements is to be transmitted at approximately a beginning of the second signal generation time period;

said second address elements is to be transmitted at approximately a fifty percent point of the second signal generation time period.

21. The bus agent of claim 19 wherein

said address strobe generation logic is to generate said first address strobe to have a first address strobe transition at substantially a first address element center point of a first address element driving window in which the first address elements are driven, and wherein

said address strobe generation logic is to generate said first address strobe to have a second transition at substantially a second address element center point of a second address element driving window in which the second address elements are driven, and wherein

said data strobe generation logic is to generate said first transition of the first data strobe to have a first transition of the first data strobe at substantially a first data

element center point of a first data element driving window in which the first data elements are driven, and wherein

said data strobe generation logic is to generate said first transition of the second data strobe to have a first transition of the second data strobe at substantially a second data element center point of a second data element driving window in which the second data elements are driven, and wherein

said data strobe generation logic is to generate said second transition of the first data strobe to have a second transition of the first data strobe at substantially a third data element center point of a third data element driving window in which the third data elements are driven, and wherein

said data strobe generation logic is to generate said second transition of the second data strobe to have a second transition of the second data strobe at substantially a fourth data element center point of a fourth data element driving window in which the fourth data elements are driven.

22. The bus agent of claim 21 wherein said first data strobe and said second data strobe are signals having out-of-phase waveforms that have an operating frequency when enabled of twice the bus clock frequency.

23. The bus agent of claim 21 wherein the first transition of the first data strobe and the second transition of the first data strobe are of a first polarity and said first data strobe

has a transition of opposite polarity after the first transition of the first data strobe and before the second transition of the first data strobe.

24. The bus agent of claim 19 wherein:

said address transmit logic is to transmit address elements at a rising edge of the bus clock signal in a first bus clock cycle of the bus clock signal and additional address elements at a 50 percent point of the first bus clock cycle, and wherein

said address strobe generation logic is to generate said first address strobe to have a first address strobe transition at a 25 percent point of the first bus clock cycle and a second address strobe transition at a 75 percent point of the first bus clock cycle, and wherein

said data transmit logic is to transmit first data elements at a second rising edge of the bus clock signal in a second bus clock cycle of the bus clock signal, second data elements at a 25 percent point of the second bus clock cycle, third data elements at a 50 percent point of the second bus clock cycle, and fourth data elements at a 75 percent point of the second bus clock cycle, and wherein

said data strobe generation logic is to generate said first data strobe and said second data strobe to have first data strobe transitions at a 12.5 percent point of the second bus clock cycle, second data strobe transitions at a 37.5 percent point of the second bus clock cycle, third data strobe transitions at a 67.5 percent point of

the second bus clock cycle, and fourth data strobe transitions at a 87.5 percent point of the second bus clock cycle.

25. The bus agent of claim 24 wherein said first data strobe and said second data strobe have offset in time waveforms, and wherein said data strobe generation logic is to generate multiple pairs of data strobes, each pair having one strobe having a waveform substantially identical to each of said first data strobe and said second data strobe.

26. The bus agent of claim 19, wherein said bus agent is to support a transaction having a plurality of phases, said plurality of phases comprising an arbitration phase, a request phase, a snoop phase, a response phase, and a data phase.

27. The bus agent of claim 19, wherein said bus agent is to support a plurality of transactions having a plurality of phases, said plurality of phases comprising an arbitration phase, a request phase, a snoop phase, a response phase, and a data phase, wherein some of said plurality of phases are optional for some transactions.

28. The bus agent of claim 27 wherein

said bus agent is capable of initiating an arbitration phase after two clocks from a prior arbitration phase and capable of receiving a block next request signal two

bus clock cycles after assertion of an address strobe signal occurs and capable of responding to said block next request signal.

29. The bus agent of claim 28 wherein:

said bus agent is capable of initiating a second request phase for a second transaction in a current clock cycle two bus clock cycles after a first request phase for a first transaction by asserting a plurality of request signals and a second transaction address strobe signal for the second transaction two bus cycles after assertion of a first transaction address strobe signal for the first transaction occurs if a most recent target ready signal active and data bus busy signal inactive observation occurs three or more bus clock cycles prior to the current clock cycle.

30. The bus agent of claim 29 wherein:

said bus agent is capable of sensing or asserting one or more of a plurality of snoop status signals for transaction N on a plurality of snoop status interfaces during a snoop phase occurring upon the later of:

three or more bus clock cycles of the bus clock signal after the assertion of an address strobe signal for transaction N; or

a most recent snoop phase for another transaction has been observed completed for zero or more clocks.

31. The bus agent of claim 30 wherein:

said bus agent is to track a plurality of a phases of a plurality of bus transactions on a bus which is a multi-phase pipelined bus, said bus agent is to track a transaction N-1 and a transaction N, wherein said bus controller is capable of asserting a response for transaction N two or more bus clock cycles after asserting a response for transaction N-1.

32. The bus agent of claim 27 wherein:

said bus agent is to track a plurality of transactions comprising a transaction N-1 and a transaction N, the bus controller being capable of asserting a target ready signal for transaction N if the bus agent is asserting the data busy signal for the transaction N-1 and deasserts the data busy signal.

33. A bus agent comprising:

address generation logic to drive two address elements in a duration of approximately one clock cycle of a bus clock signal, said address generation logic to generate a first address strobe to have a first address strobe transition at substantially a first address element center point of a first address element driving window in which the first address elements are driven, said address generation logic to generate said first address strobe to have a second transition at substantially a second address

element center point of a second address element driving window in which the second address elements are driven;

data generation logic to drive four data elements in a second duration of approximately one clock cycle of the bus clock signal, said data generation logic to generate a first data strobe to have a first transition of the first data strobe at substantially a first data element center point of a first data element driving window in which a first data element is driven, and wherein said data generation logic is to generate a second data strobe to have a first transition of the second data strobe at substantially a second data element center point of a second data element driving window in which a second data element is driven, and wherein said data generation logic is to generate said first data strobe to have a second transition of the first data strobe at substantially a third data element center point of a third data element driving window in which a third data element is driven, and wherein said data generation logic is to generate said second data strobe to have a second transition of the second data strobe at substantially a fourth data element center point of a fourth data element driving window in which a fourth data element is driven.

34. The bus agent of claim 33 wherein a first transition of the first data strobe and a second transition of the first data strobe are of a first polarity and said first data strobe

has a transition of opposite polarity after the first transition of the first data strobe and before the second transition of the first data strobe.

35. The bus agent of claim 33 wherein said first data strobe and said second data strobe have a frequency of twice a bus clock signal frequency.

36. The bus agent of claim 33 wherein said first and second transitions of the first and second data strobes are all either rising or falling edges.

37. The bus agent of claim 34 wherein said first address strobe transition is of a first type of either rising or falling and said second address strobe transition is of a second type, being the other of rising or falling, opposite the first address strobe transition.

38. The bus agent of claim 37 further comprising:

a control interface to transmit a common clock control signal in an address phase that also includes generation of said two address elements, and to generate a second common clock control signal in a data phase that also includes operation of said four data elements.

39. A bus agent comprising:

a control interface to drive control signals at a bus clock frequency;

an address bus interface to drive address elements at twice the bus clock frequency, said address elements to be synchronized to an address strobe signal, a first transition of the address strobe signal being driven at approximately a center point of a first address element, a second transition of the address strobe being driven at approximately a center point of a second address element;

a data bus interface to drive data elements at four times the bus clock frequency, said data elements to be synchronized to a plurality of data strobe signals, said plurality of data strobe signals providing a transition at approximately a center point of each data element.

40. A bus agent comprising:

a control interface to drive a control signal at a clock frequency;

an address bus interface to transmit address elements at twice the clock frequency, said address bus interface to drive a substantially centered address strobe transition for each address element;

a data bus interface to transmit data elements at four times the clock frequency, said data bus interface to drive a substantially centered data strobe transition for each data element, wherein

said bus agent is capable of initiating an arbitration phase after two clocks from a prior arbitration phase and capable of receiving a block next request signal two

bus clock cycles after assertion of an address strobe signal occurs and capable of responding to said block next request signal;

said bus agent is capable of initiating a second request phase for a second transaction in a current clock cycle two bus clock cycles after a first request phase for a first transaction by asserting a plurality of request signals and a second transaction address strobe signal for the second transaction two bus cycles after assertion of a first transaction address strobe signal for the first transaction occurs if a most recent target ready signal active and data bus busy signal inactive observation occurs three or more bus clock cycles prior to the current clock cycle;

said bus agent is capable of sensing or asserting one or more of a plurality of snoop status signals for transaction N on a plurality of snoop status interfaces during a snoop phase occurring upon a later one of:

three or more bus clock cycles of a bus clock signal after the assertion of an address strobe signal for transaction N; or

a most recent snoop phase for another transaction has been observed completed for zero or more clocks.

41. The bus agent of claim 40 wherein

said bus agent is to track a plurality of a phases of a plurality of bus transactions on a bus which is a multi-phase pipelined bus, said bus agent to track a transaction N-1 and a transaction N, wherein said bus agent is capable of asserting a response for

transaction N in a current cycle two or more bus clock cycles after asserting a response for transaction N-1 if a most recent target ready signal active and data bus busy signal inactive observation occurred three or more clock cycles prior to the current cycle.

42. The bus agent of claim 41 wherein

said bus agent is capable of asserting the target ready signal for transaction N if the bus agent is asserting the data busy signal for the transaction N-1 and deasserts the data busy signal.

43. A bus agent comprising:

a bus controller capable of initiating an arbitration phase after two clocks from a prior arbitration phase and capable of receiving a block next request signal two bus clock cycles after assertion of an address strobe signal and capable of responding to said block next request signal;

said bus controller is capable of initiating a second request phase for a second transaction in a current clock cycle two bus clock cycles after a first request phase for a first transaction by asserting a plurality of request signals and a second transaction address strobe signal for the second transaction two bus cycles after assertion of a first transaction address strobe signal for the first transaction occurs if a most recent target ready signal active and data bus busy signal inactive

observation occurs three or more bus clock cycles prior to the current clock cycle;

said bus controller being capable of sensing or asserting one or more of a plurality of snoop status signals for transaction N on a plurality of snoop status interfaces during a snoop phase occurring upon a later one of:

three or more bus clock cycles of a bus clock signal after the assertion of an address strobe signal for transaction N; or

a most recent snoop phase for another transaction has been observed completed for zero or more clocks.

44. The bus agent of claim 43 wherein

said bus controller is to track a plurality of a phases of a plurality of bus transactions, said bus controller to track a transaction N-1 and a transaction N, wherein said bus controller is capable of asserting a response for transaction N in a current cycle two or more bus clock cycles after asserting a response for transaction N-1 if a most recent target ready signal active and data bus busy signal inactive observation occurred three or more bus clock cycles prior to the current cycle;

said bus controller being capable of asserting a target ready signal for transaction P if the bus agent is asserting a data busy signal for the transaction P-1 and deasserts the data busy signal.

45. The bus agent of claim 43 further comprising:

a control interface to operate at a clock frequency;

an address bus interface to transmit address elements at twice the clock frequency during a request phase, said address bus interface to drive a substantially centered address strobe transition for each address element, said address bus interface to drive ;

a data bus interface to transmit data elements at four times the clock frequency during a data phase, said data bus interface to drive a substantially centered data strobe transition for each data element.

46. The bus agent of claim 44 wherein said bus controller is to support a plurality of transactions having a plurality of phases, said plurality of phases comprising an arbitration phase, a request phase, a snoop phase, a response phase, and a data phase, wherein some of said plurality of phases are optional for some transactions.

47. A bus agent comprising:

a bus controller to track a plurality of a phases of a plurality of bus transactions, said bus controller to track a transaction N-1 and a transaction N, wherein said bus controller is capable of asserting a response for transaction N two or more bus clock cycles after asserting a response for transaction N-1;

said bus controller being capable of asserting a target ready signal for transaction P if the bus agent is asserting a data busy signal for the transaction P-1 and deasserts

the data busy signal.

48. The bus agent of claim 47 further comprising:

an address bus interface to transmit address elements at twice the clock frequency during the request phase, said address bus interface to drive a substantially centered address strobe transition for each address element, said address bus interface to drive ;

a data bus interface to transmit data elements at four times the clock frequency during the data phase, said data bus interface to drive a substantially centered data strobe transition for each data element.

49. A system comprising:

a processor comprising:

a processor bus controller capable of initiating an arbitration phase after two clocks from a prior arbitration phase and capable of receiving a block next request signal two bus clock cycles after assertion of an address strobe signal occurs and capable of responding to said block next request signal;

said processor bus controller being capable of initiating a second request phase in a current clock cycle for a second transaction two clocks after a first request phase for a first transaction by asserting a plurality of request signals and a second transaction address strobe signal for the second transaction two bus

cycles after assertion of a first transaction address strobe signal for the first transaction occurs if a most recent target ready signal active and data bus busy signal inactive observation occurred three or more bus clock cycles prior to the current clock cycle;

a chipset comprising:

a chipset bus controller to track a plurality of a phases of a plurality of bus transactions, said chipset bus controller to track a transaction N-1 and a transaction N, wherein said chipset bus controller is capable of asserting a response for transaction N in a current clock cycle two or more bus clock cycles after asserting a response for transaction N-1 if a most recent target ready signal active and data bus busy signal inactive observation occurred three or more clocks prior to the current cycle;

said chipset bus controller being capable of sensing or asserting one or more of a plurality of snoop status signals for transaction N on a plurality of snoop status interfaces during a snoop phase occurring upon a later one of:

three or more bus clock cycles of a bus clock signal after the assertion of an address strobe signal for transaction N; or

a most recent snoop phase for another transaction has been observed completed for zero or more clock;

said chipset bus controller being capable of asserting a target ready signal for transaction N if the bus agent is asserting a data busy signal for the transaction

N-1 and deasserts the data busy signal.

50. The system of claim 49 wherein each of said processor and said chipset further comprises:

a control interface to operate at a clock frequency;

an address bus interface to transmit address elements at twice the clock frequency, said address bus interface to drive a substantially centered address strobe transition for each address element;

a data bus interface to transmit data elements at four times the clock frequency, said data bus interface to drive a substantially centered data strobe transition for each data element.

51. A method comprising:

generating a first address element and a second address element in a first duration substantially equivalent in duration to a bus clock cycle of a bus clock signal;

generating an address strobe having a first address strobe transition substantially centered on said first address element and having second address strobe transition substantially centered on said second address element;

generating a first data element, a second data element, a third data element, and a fourth data element in a second duration substantially equivalent in duration to the bus clock cycle of the bus clock signal;

generating a plurality of data strobes to provide a data strobe transition substantially centered on each data element.

52. The method of claim 51 further comprising:

generating a common clock address strobe control signal according to a common clock protocol during a bus clock cycle in which transfer of said first and second address elements commences.

53. The method of claim 52 wherein said first address strobe transition has a first polarity and said second address strobe transition has a second polarity.

54. The method of claim 53 further comprising:

asserting a data bus busy signal for an N-1th transaction in a first bus clock cycle;

asserting a target ready signal for an Nth transaction in a second bus clock cycle which is adjacent to said first bus clock cycle only if a data bus busy signal is deasserted in the second bus cycle and if a bus agent deasserting the data bus busy signal also asserts the target ready signal.

55. An article comprising a machine readable medium that carries data representing an integrated circuit comprising:

a control interface to drive a control signal at a clock frequency;

an address bus interface to drive address elements at twice the clock frequency, said address bus interface to drive a substantially centered address strobe transition for each address element;

a data bus interface to drive data elements at four times the clock frequency, said data bus interface to drive a substantially centered data strobe transition for each data element.

56. The article of claim 55 carrying further data representing the integrated circuit, wherein said address bus interface is to drive a first address strobe at the clock frequency, said first address strobe having a first address strobe transition of a first polarity to be substantially centered on a first address element and a second address strobe transition of a second polarity to be substantially centered on a second address element, the second address element being consecutive to the first address element, and wherein said data bus interface is to drive four consecutive data elements and a first data strobe and a second data strobe, and wherein a first edge of a first type of the first data strobe is to be substantially centered on a first data element, a first edge of the first polarity of the second data strobe is to be substantially centered on the second data element, a second edge of the first polarity of the first data strobe is to be substantially centered on the third data element, and a second edge of the first polarity of the second data strobe is to be substantially centered on the fourth data element.

57. The article of claim 56 carrying further data representing the integrated circuit, which comprises a bus agent, said bus agent is to track a plurality of transactions comprising a transaction N-1 and a transaction N, the bus agent being capable of asserting the target ready signal for transaction N if the bus agent is asserting the data busy signal for the transaction N-1 and deasserts the data busy signal.

58. The article of claim 56 carrying further data representing the integrated circuit, which comprises a bus controller to track a plurality of a phases of a plurality of bus transactions, said bus controller to track a transaction N-1 and a transaction N, wherein said bus controller is capable of asserting a response for transaction N in a current cycle two or more bus clock cycles after asserting a response for transaction N-1 if a most recent target ready signal active and data bus busy signal inactive observation occurred three or more bus cycles prior to the current cycle, said bus controller being capable of asserting a target ready signal for transaction P if the bus agent is asserting a data busy signal for the transaction P-1 and deasserts the data busy signal.

59. An article comprising a machine readable carrier medium carrying data which, when loaded into a computer system memory in conjunction with simulation routines,

provides functionality of a model comprising:

a bus controller capable of initiating an arbitration phase after two clocks from a prior arbitration phase and capable of receiving a block next request signal two bus clock cycles after assertion of an address strobe signal and capable of responding to said block next request signal;

said bus controller is capable of initiating a second request phase for a second transaction in a current clock cycle two bus clock cycles after a first request phase for a first transaction by asserting a plurality of request signals and a second transaction address strobe signal for the second transaction two bus cycles after assertion of a first transaction address strobe signal for the first transaction occurs if a most recent target ready signal active and data bus busy signal inactive observation occurs three or more bus clock cycles prior to the current clock cycle;

said bus controller being capable of sensing or asserting one or more of a plurality of snoop status signals for transaction N on a plurality of snoop status interfaces during a snoop phase occurring upon a later one of:

three or more bus clock cycles of a bus clock signal after the assertion of an address strobe signal for transaction N; or

a most recent snoop phase for another transaction has been observed completed for zero or more clocks.

60. The article of claim 59 wherein the model further comprises:

a control interface to operate at a clock frequency;

an address bus interface to transmit address elements at twice the clock frequency during a request phase, said address bus interface to drive a substantially centered address strobe transition for each address element, said address bus interface to drive ;

a data bus interface to transmit data elements at four times the clock frequency during a data phase, said data bus interface to drive a substantially centered data strobe transition for each data element.

61. An article comprising a machine readable carrier medium carrying data which, when loaded into a computer system memory in conjunction with simulation routines, provides functionality of a model comprising:

a bus controller to track a plurality of a phases of a plurality of bus transactions, said bus controller to track a transaction N-1 and a transaction N, wherein said bus controller is capable of asserting a response for transaction N in a current cycle two or more bus clock cycles after asserting a response for transaction N-1 if a most recent target ready signal active and data bus busy signal inactive observation occurred three or more bus cycles prior to the current cycle;

said bus controller being capable of asserting a target ready signal for transaction

P if the bus agent is asserting a data busy signal for the transaction P-1 and deasserts the data busy signal.

62. The article of claim 61 wherein the model further comprises:

a control interface to operate at a clock frequency;

an address bus interface to transmit address elements at twice the clock frequency during a request phase, said address bus interface to drive a substantially centered address strobe transition for each address element, said address bus interface to drive ;

a data bus interface to transmit data elements at four times the clock frequency during a data phase, said data bus interface to drive a substantially centered data strobe transition for each data element.